FIG. 1

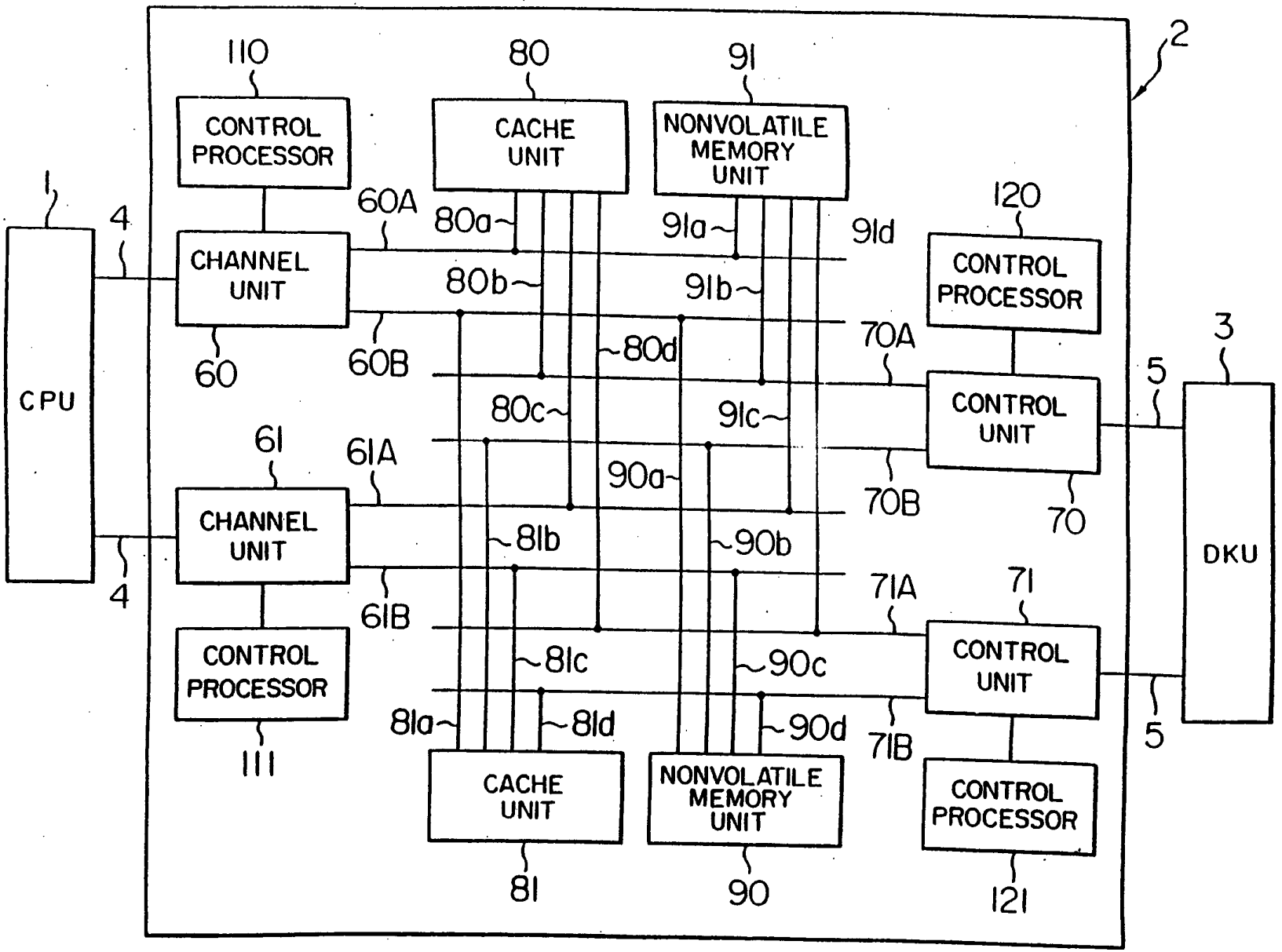

2
110
80
91
CONTROL PROCESSOR
CACHE UNIT
NONVOLATILE MEMORY UNIT
1
4
60A
80a
91a
91d
120
CHANNEL UNIT
80b
91b
CONTROL PROCESSOR
60
60B
80d
70A
3
CPU
5
80c
91c
61
61A
CONTROL UNIT
90a
70B
DKU
CHANNEL UNIT
81b
90b
70
4
61B
71A
71
CONTROL PROCESSOR
81c
90c
CONTROL UNIT
81a
81d
90d
71B
5
111
CACHE UNIT
NONVOLATILE MEMORY UNIT
CONTROL PROCESSOR
81
90
121

FIG. 2

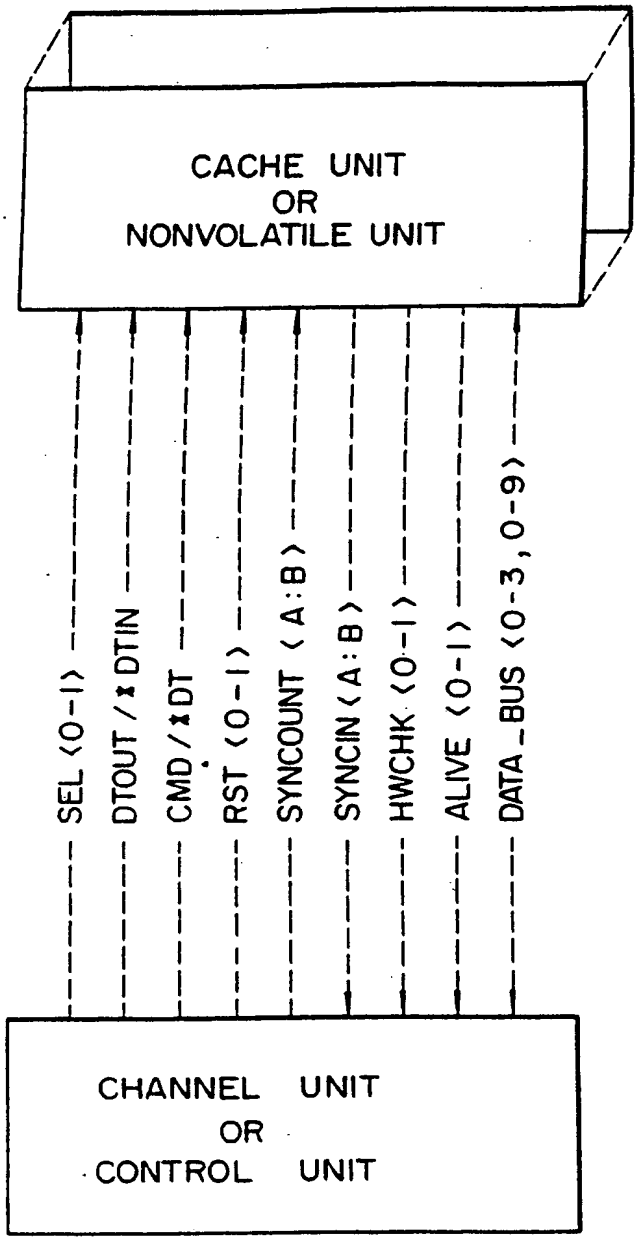

CACHE UNIT
OR
NONVOLATILE UNIT
SEL ⟨0-1⟩
DTOUT / ⁑DTIN
CMD / ⁑DT
RST ⟨0-1⟩
SYNCOUNT ⟨A:B⟩
SYNCIN ⟨A:B⟩
HWCHK ⟨0-1⟩
ALIVE ⟨0-1⟩
DATA_BUS ⟨0-3, 0-9⟩
CHANNEL UNIT
OR
CONTROL UNIT

FIG. 3

DATA BUS PROTOCOL

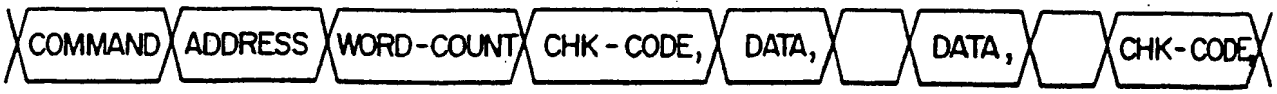


FIG. 4

DATA BUS MODE

DUOUT / ¤DTIN	CMD / ¤DT	BUS MODE
1	1	TRANSFER COMMAND
1	0	TRANSFER WRITE DATA
0	1	TRANSFER STATUS
0	0	TRANSFER READ DATA

FIG. 5

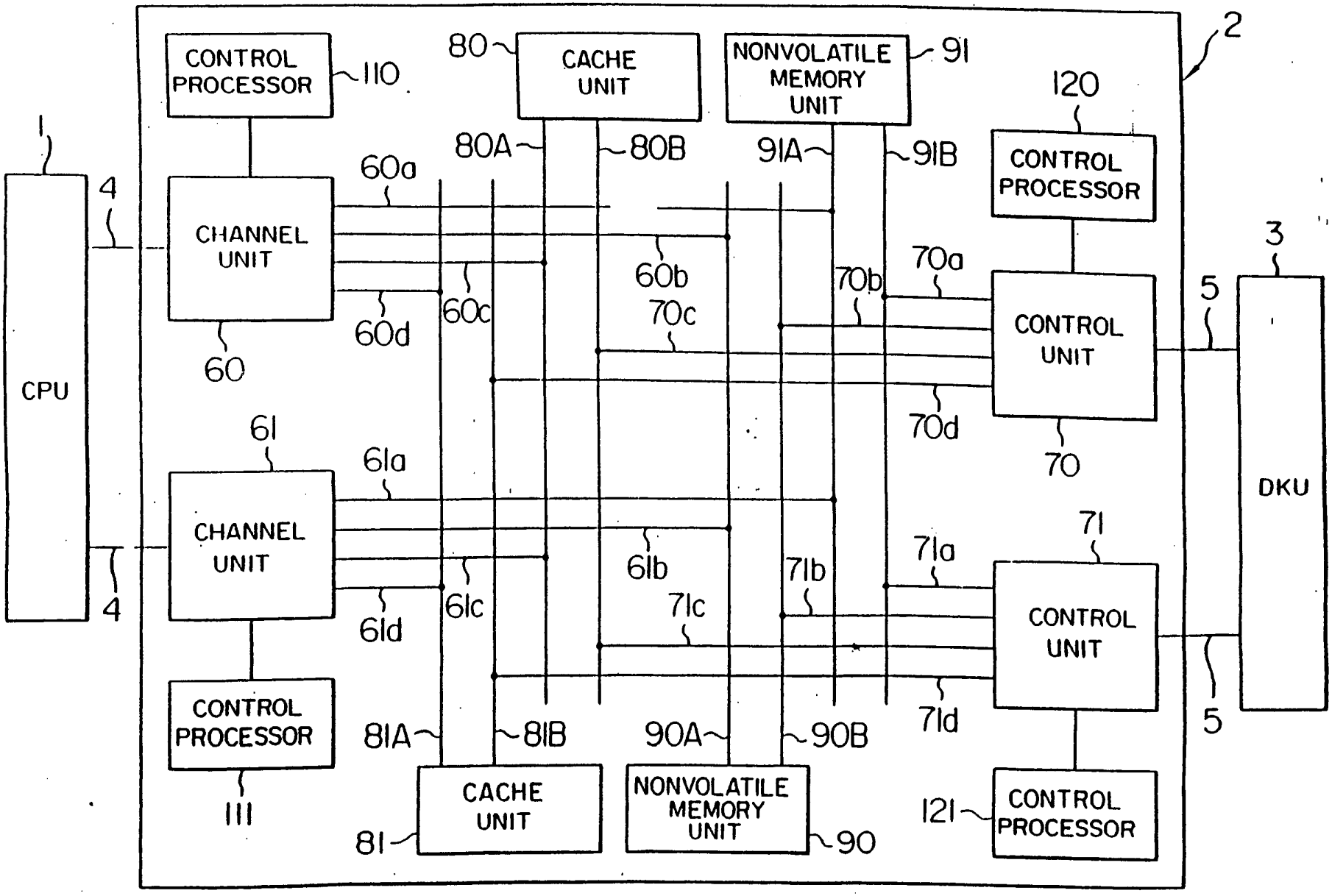

CONTROL PROCESSOR
110
80
CACHE UNIT
NONVOLATILE MEMORY UNIT
91
120
2
1
4
80A
80B
91A
91B
CONTROL PROCESSOR
60a
CHANNEL UNIT
60b
70a
70b
3
60c
70c
5
60d
CONTROL UNIT
60
70d
70
61
61a
DKU
CHANNEL UNIT
71
71a
61b
71b
CPU
61c
71c
CONTROL UNIT
61d
71d
CONTROL PROCESSOR
81A
81B
90A
90B
5
CACHE UNIT
NONVOLATILE MEMORY UNIT
111
81
90
121
CONTROL PROCESSOR

FIG. 6

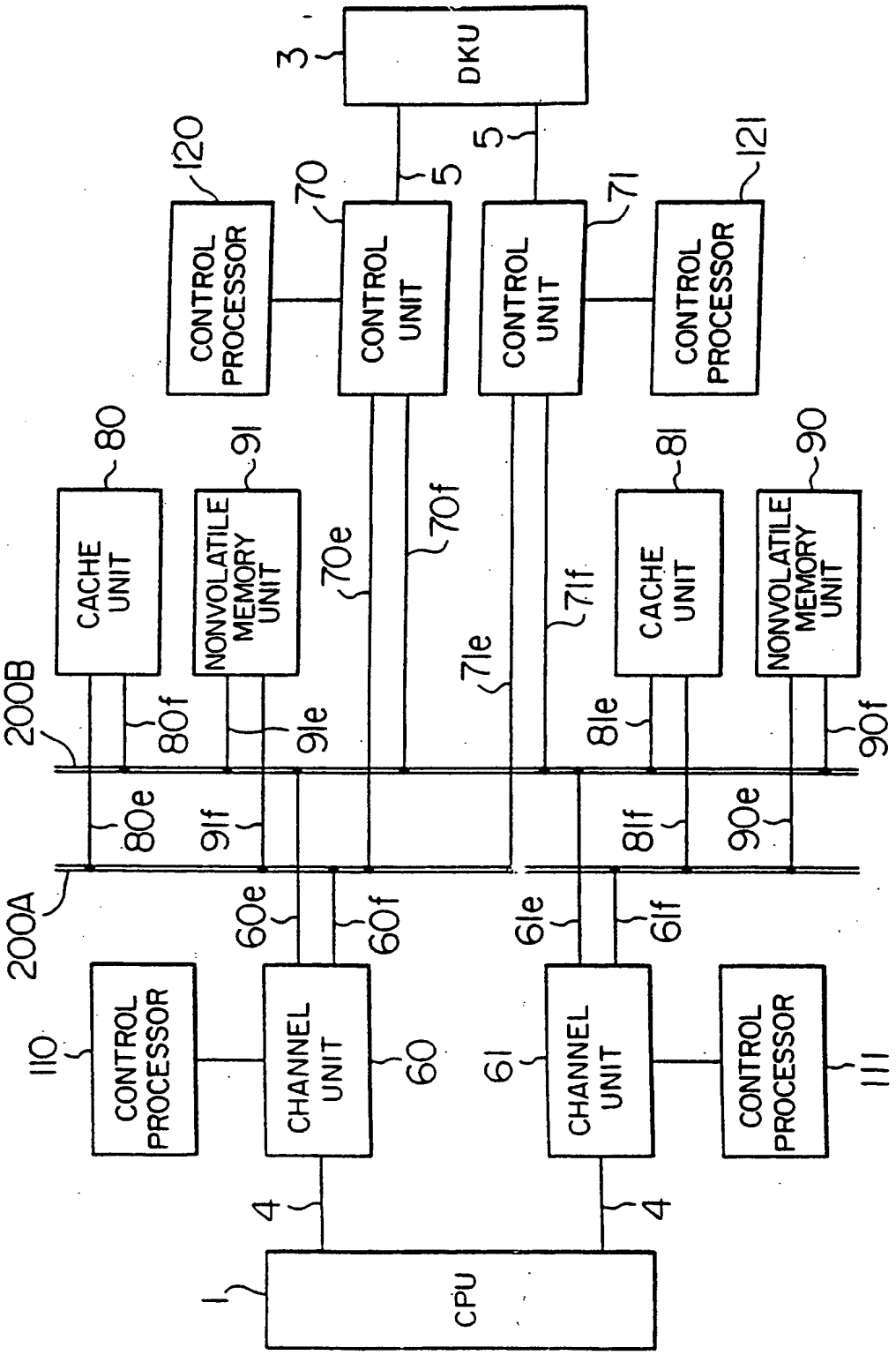
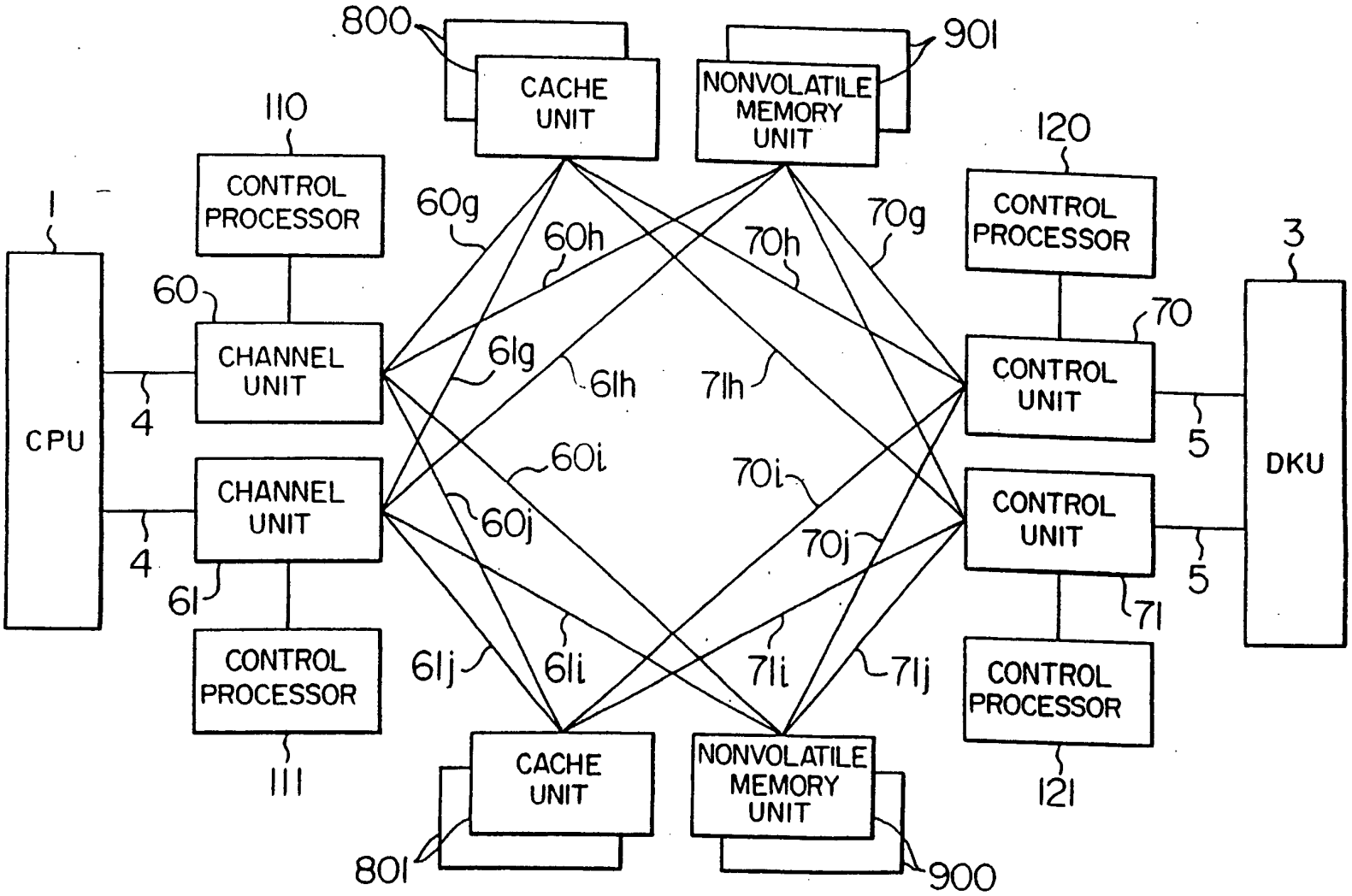

CPU
1
4
4
CONTROL PROCESSOR
110
CHANNEL UNIT
60
CHANNEL UNIT
61
CONTROL PROCESSOR
111
200A
60e
60f
61e
61f
200B
80e
91f
81f
90e
CACHE UNIT
80
NONVOLATILE MEMORY UNIT
91
CACHE UNIT
81
NONVOLATILE MEMORY UNIT
90
80f
91e
81e
90f
70e
70f
71e
71f
CONTROL PROCESSOR
120
CONTROL UNIT
70
CONTROL UNIT
71
CONTROL PROCESSOR
121
5
5
DKU
3

FIG. 7


800
CACHE UNIT
901
NONVOLATILE MEMORY UNIT
110
CONTROL PROCESSOR
120
CONTROL PROCESSOR
1
CPU
60g
60h
70h
70g
3
60
CHANNEL UNIT
61g
61h
71h
70
CONTROL UNIT
4
5
DKU
60i
70i
CHANNEL UNIT
60j
70j
CONTROL UNIT
4
5
61
71
CONTROL PROCESSOR
61j
61i
71i
71j
CONTROL PROCESSOR
111
121
CACHE UNIT
NONVOLATILE MEMORY UNIT
801
900